Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. An SOC comprising:

a processor for controlling operation of the SOC;

a high-speed bridge circuit connected to the processor, the high-speed bridge circuit being used to control signal transmission between the processor and a high-speed peripheral device connected to the high-speed bridge circuit;

a low-speed bridge circuit connected to the high-speed bridge circuit, the low-speed bridge circuit being used to control signal transmission between the high-speed bridge circuit and a first low-speed peripheral device connected to the low-speed bridge circuit; and

an expansion port connected to the high-speed bridge circuit, the expansion port being used to connect to an expanding bridge circuit, the expanding bridge circuit being externally connected to the SOC and controlling signal transmission between the high-speed bridge circuit and at least a second low-speed peripheral device connected to the expanding bridge circuit.

[c2] 2. The SOC of claim 1 wherein the processor comprises a

RISC processor.

[c3] 3. The SOC of claim 1 further comprising:
a multiplexer comprising:
an input connected to the expansion port;
a first output connected to the high-speed bridge circuit; and
a second output connected to the low-speed bridge circuit.

[c4] 4. The SOC of claim 3 wherein the multiplexer connects the input and the first output when the expanding bridge circuit is connected to the expansion port.

[c5] 5. The SOC of claim 3 wherein the expansion port is selectively connected to an input/output port of the SOC or to the expanding bridge circuit.

[c6] 6. The SOC of claim 5 wherein the multiplexer connects the input and the second output when the expansion port is connected to the input/output port.

[c7] 7. The SOC of claim 1 wherein the low-speed bridge circuit is connected to a first input/output port, and the expanding bridge circuit is connected to a second input/output port; wherein the first input/output port is used to connect to the first low-speed peripheral device, and the second input/output port is used to connect to the

second low-speed peripheral device.

[c8] 8. The SOC of claim 1 wherein the expansion port is connected to the expanding bridge circuit using a bus connector.

[c9] 9. The SOC of claim 8 wherein the bus connector comprises a V-link bus.

[c10] 10. The SOC of claim 8 wherein the bus connector comprises a PCI bus.

[c11] 11. The SOC of claim 1 wherein the expanding bridge circuit comprises a south bridge circuit of x86 architecture.

[c12] 12. The SOC of claim 1 wherein the SOC is installed in a package, and the expansion port comprises a plurality of pinouts of the package.

[c13] 13. The SOC of claim 1 wherein the SOC is utilized in an embedded system.